Reconfigurable Devices in the 21st Century

An Evolutionary Perspective

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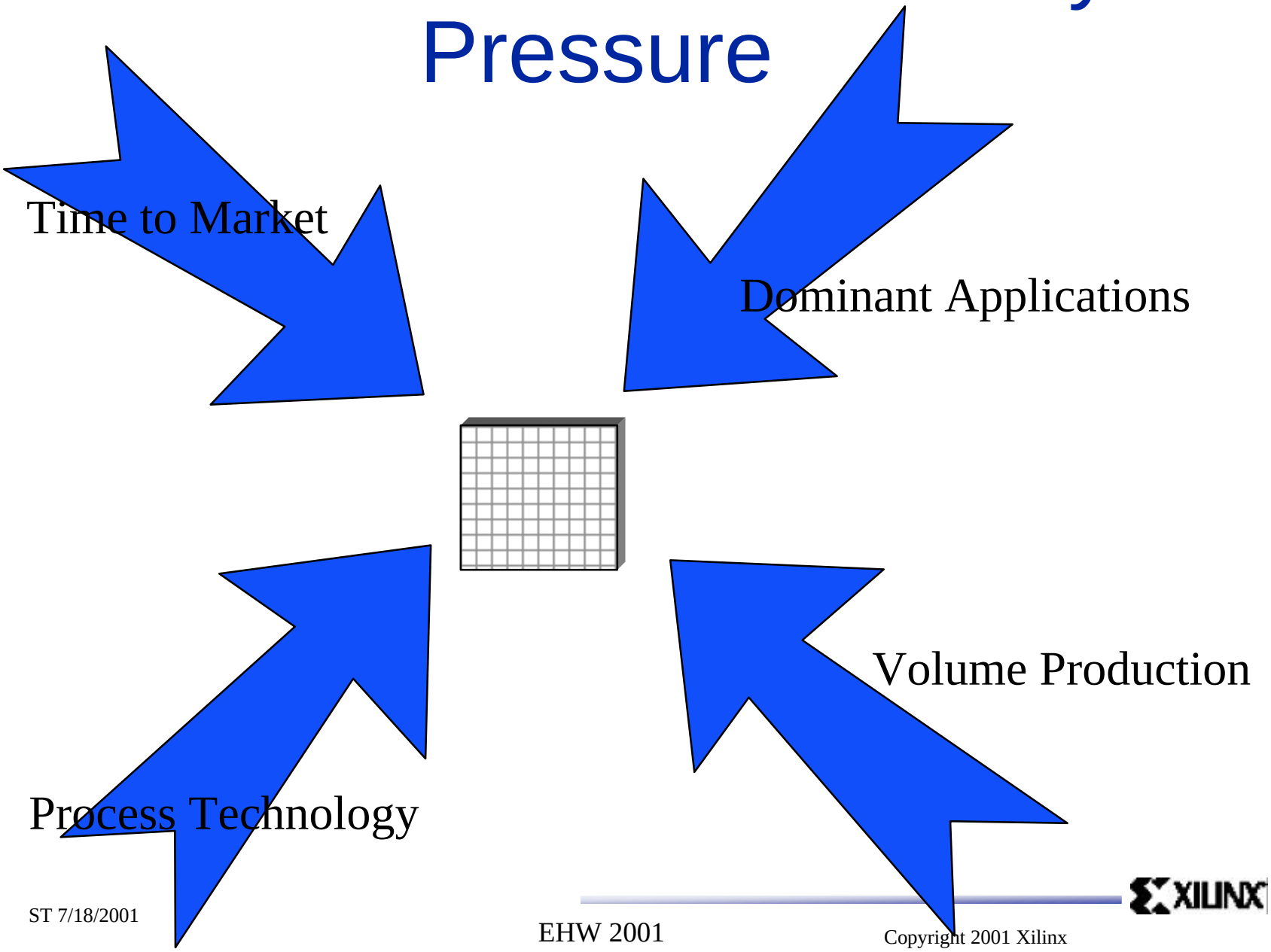
Principal Engineer

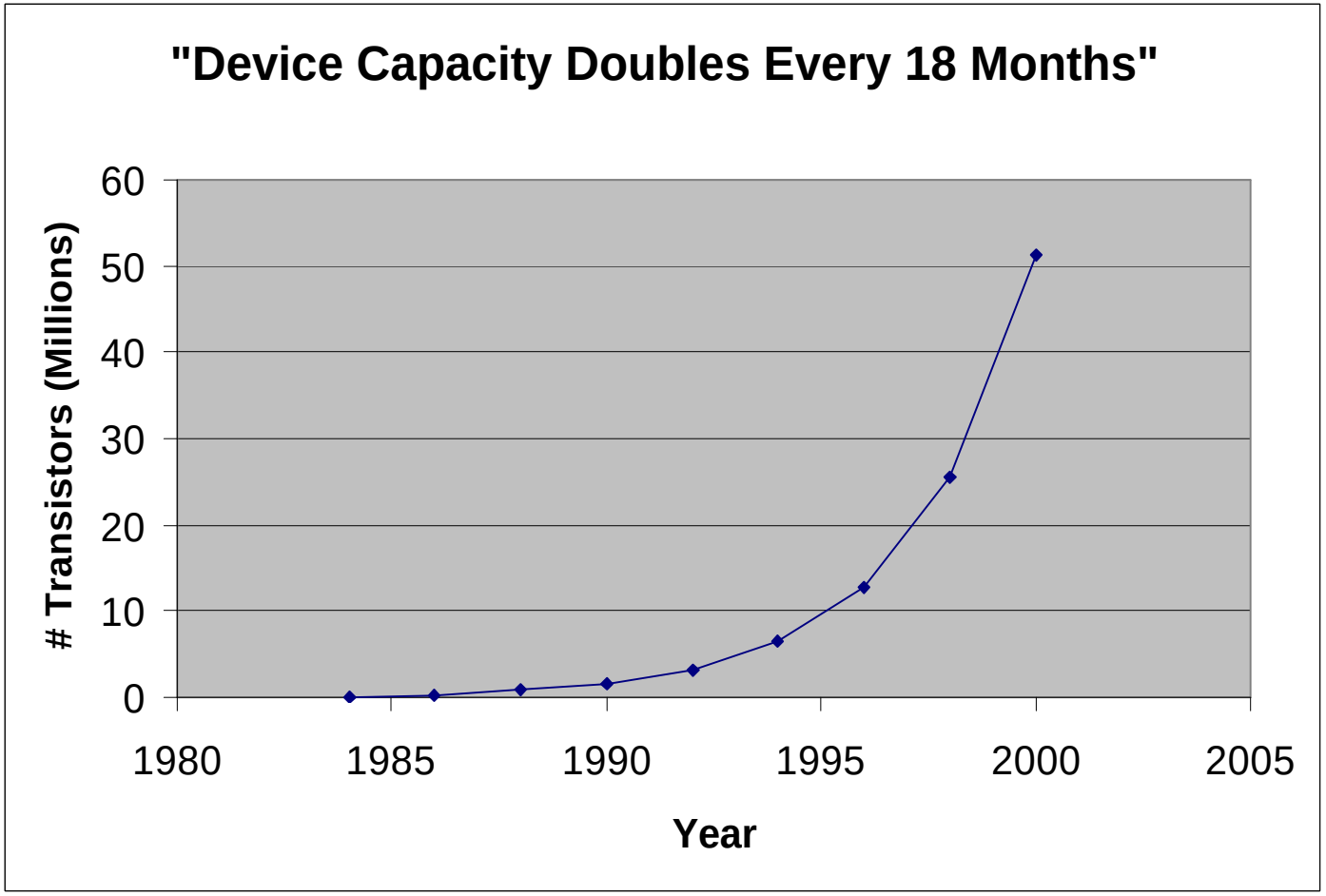
FPGA Evolution

- **Part 1. Environment**
  - Primordial soup, ice ages and global warming
- Part 2. Development
- Part 3. Focus on Reconfiguration
- Part 4. Looking Ahead

Environment: Evolutionary Pressure

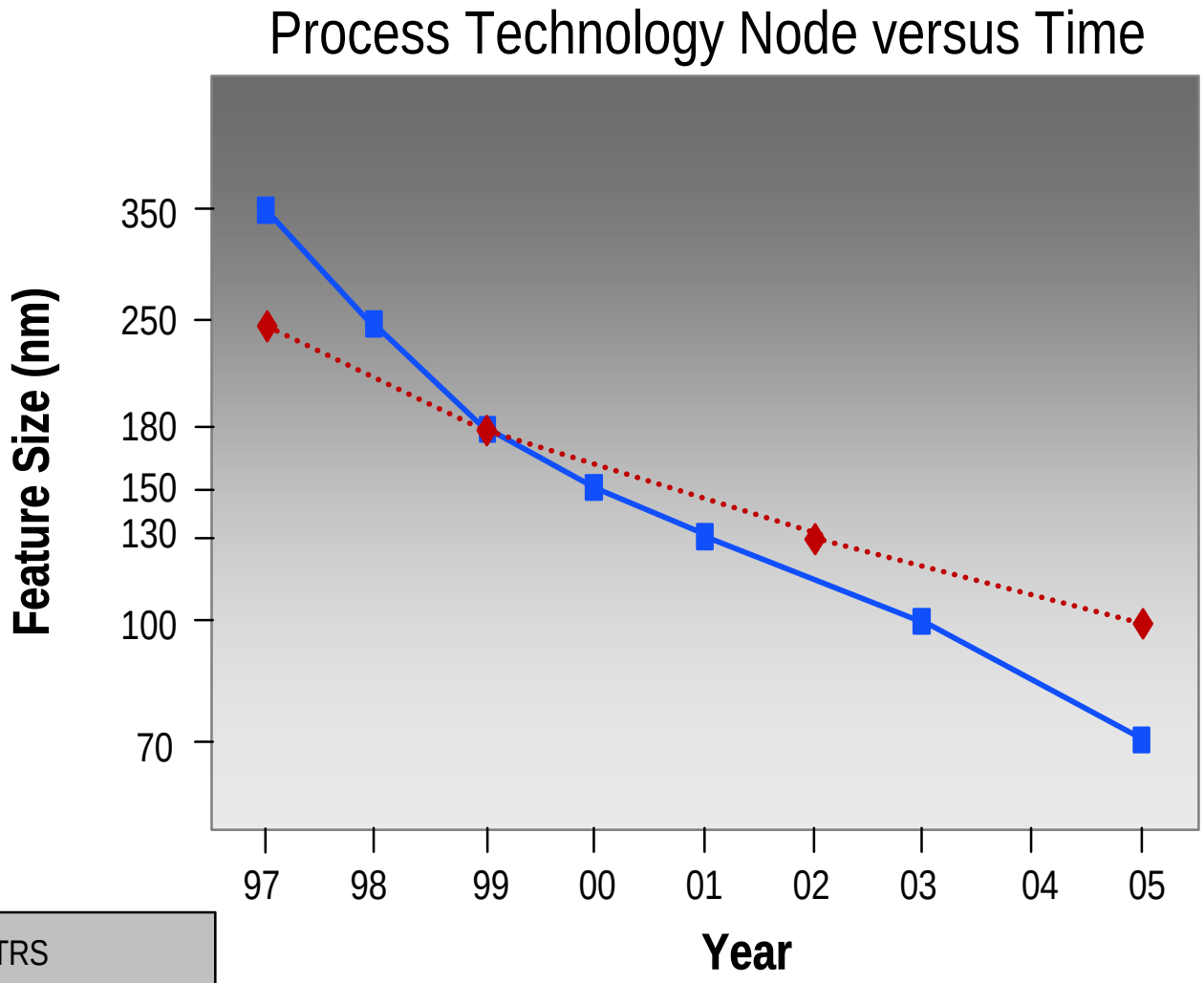


The Primordial Soup: Moore's Law

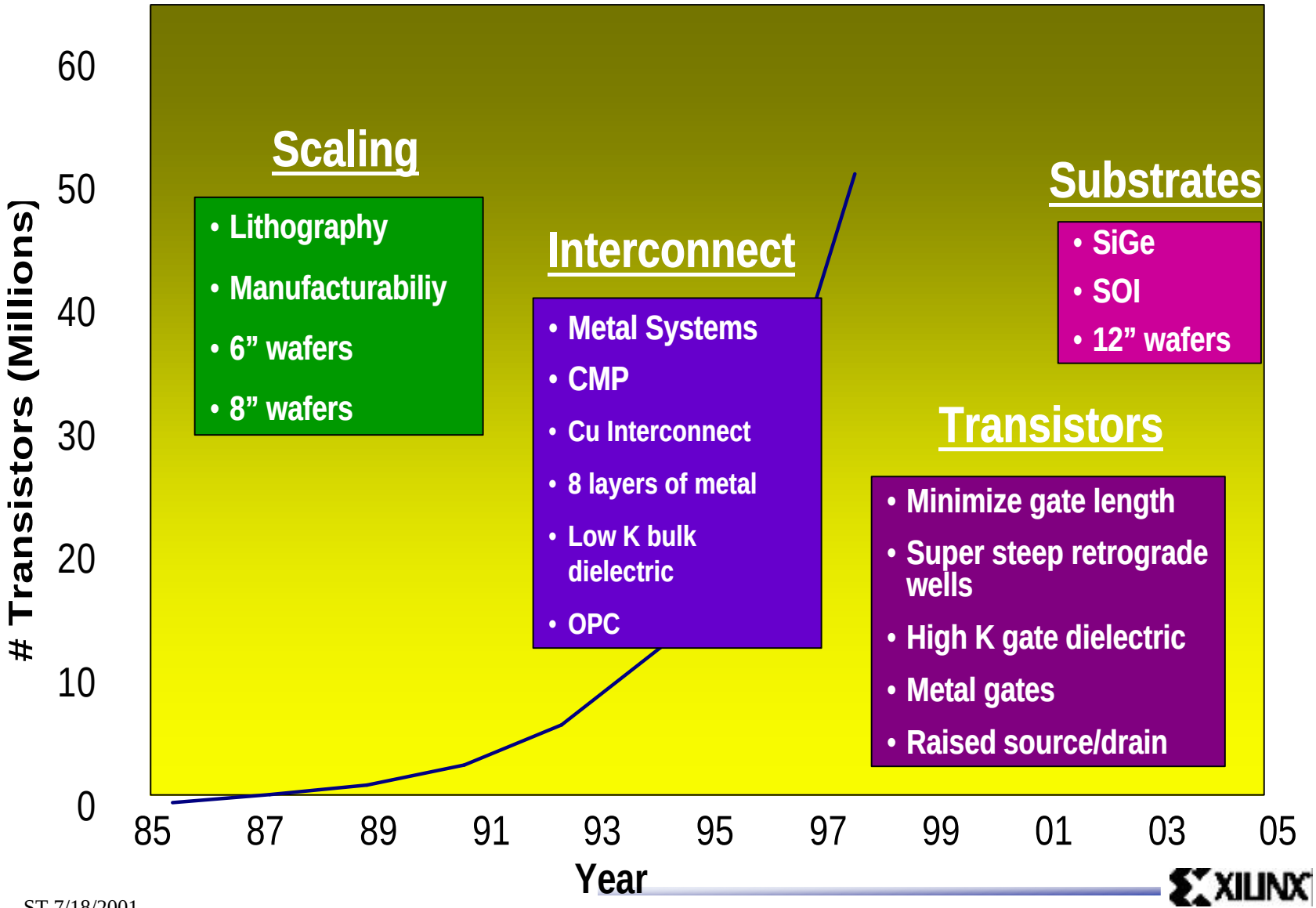


Source: SIA

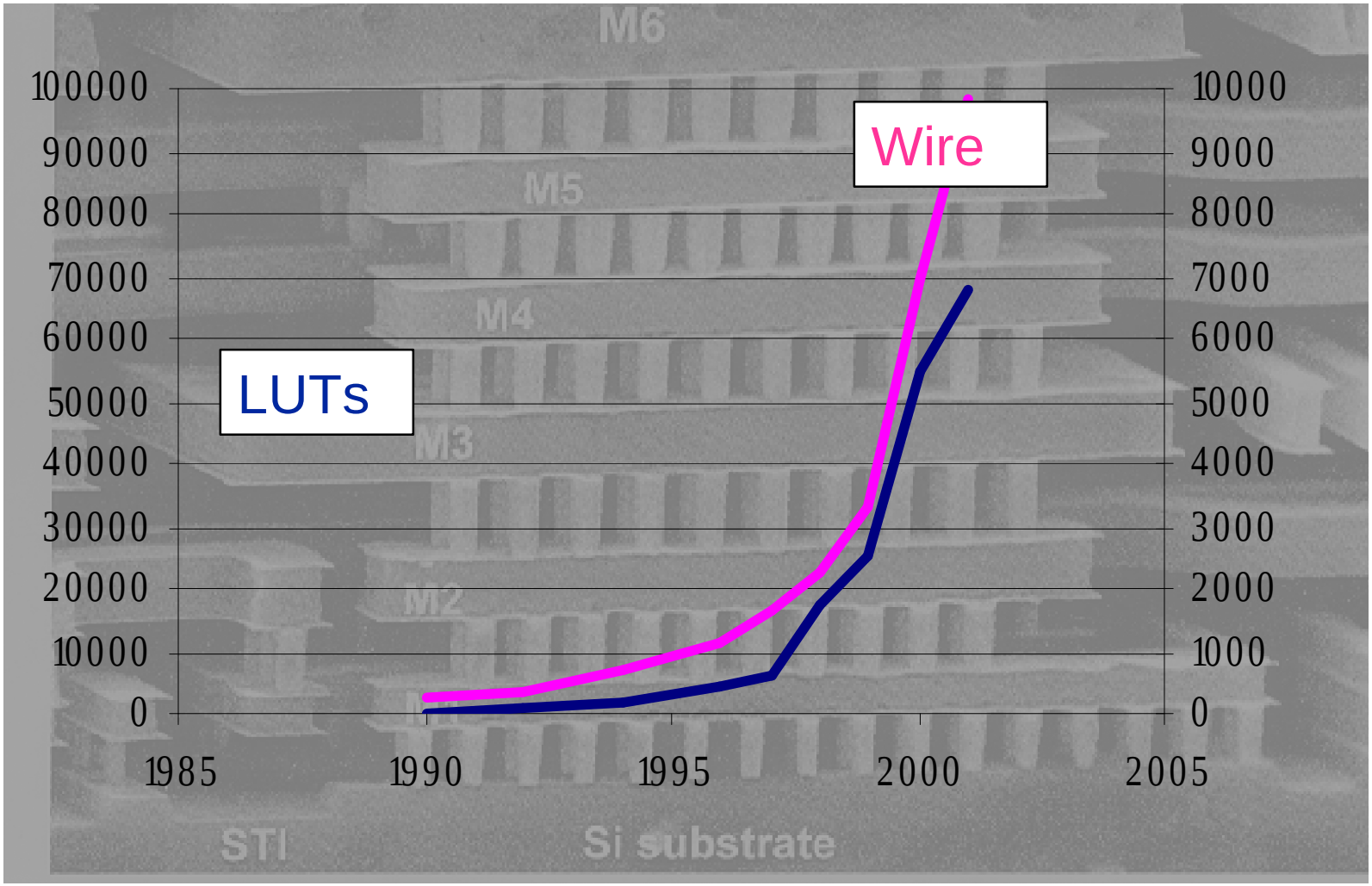
FPGAs: Ahead of the Curve



Major Process Focus

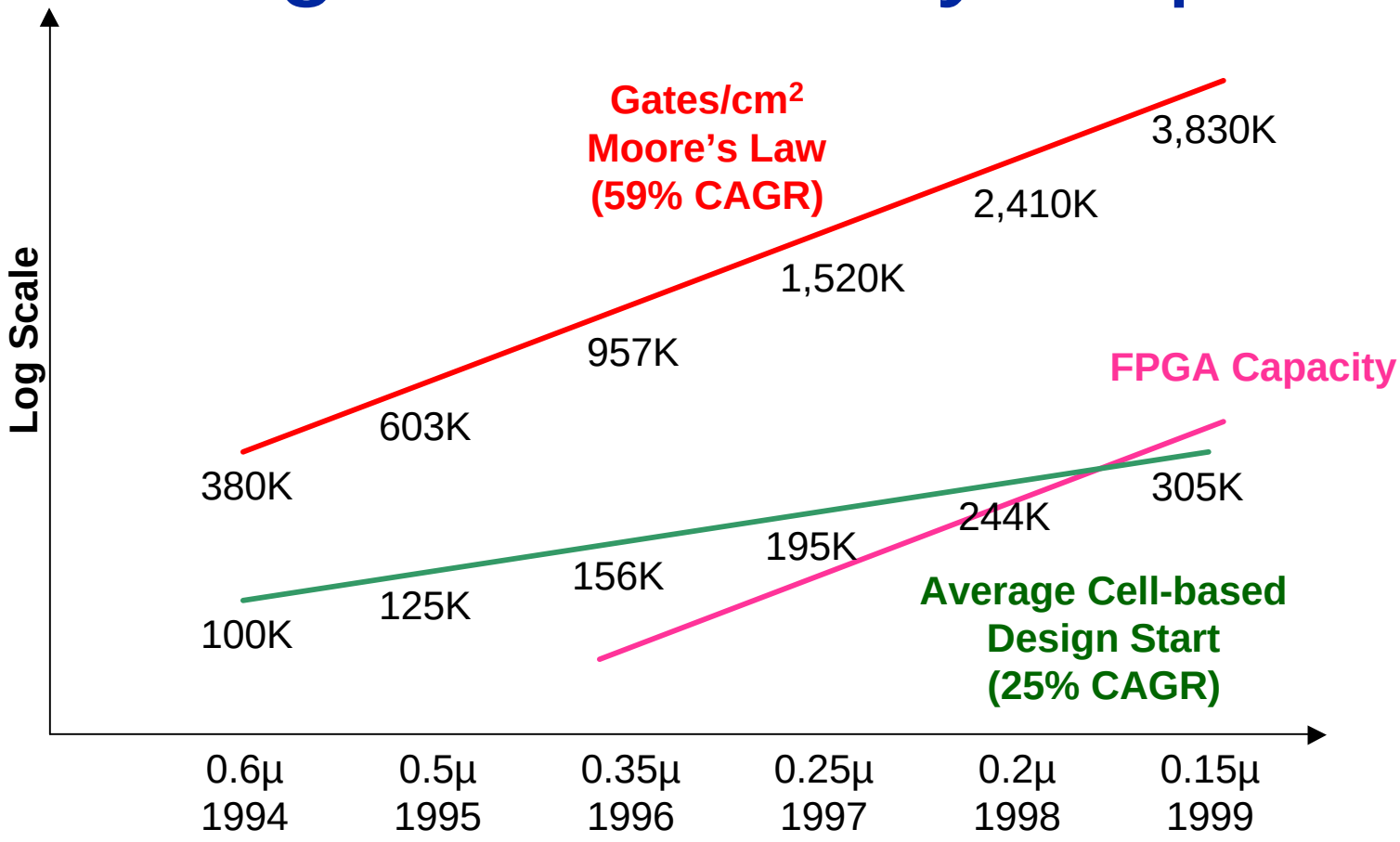


Catastrophism: Major Environment Change in the 90s



Courtesy and Copyright of UMC

Time to Market: Design Productivity Gap



Source: VLSI Technology

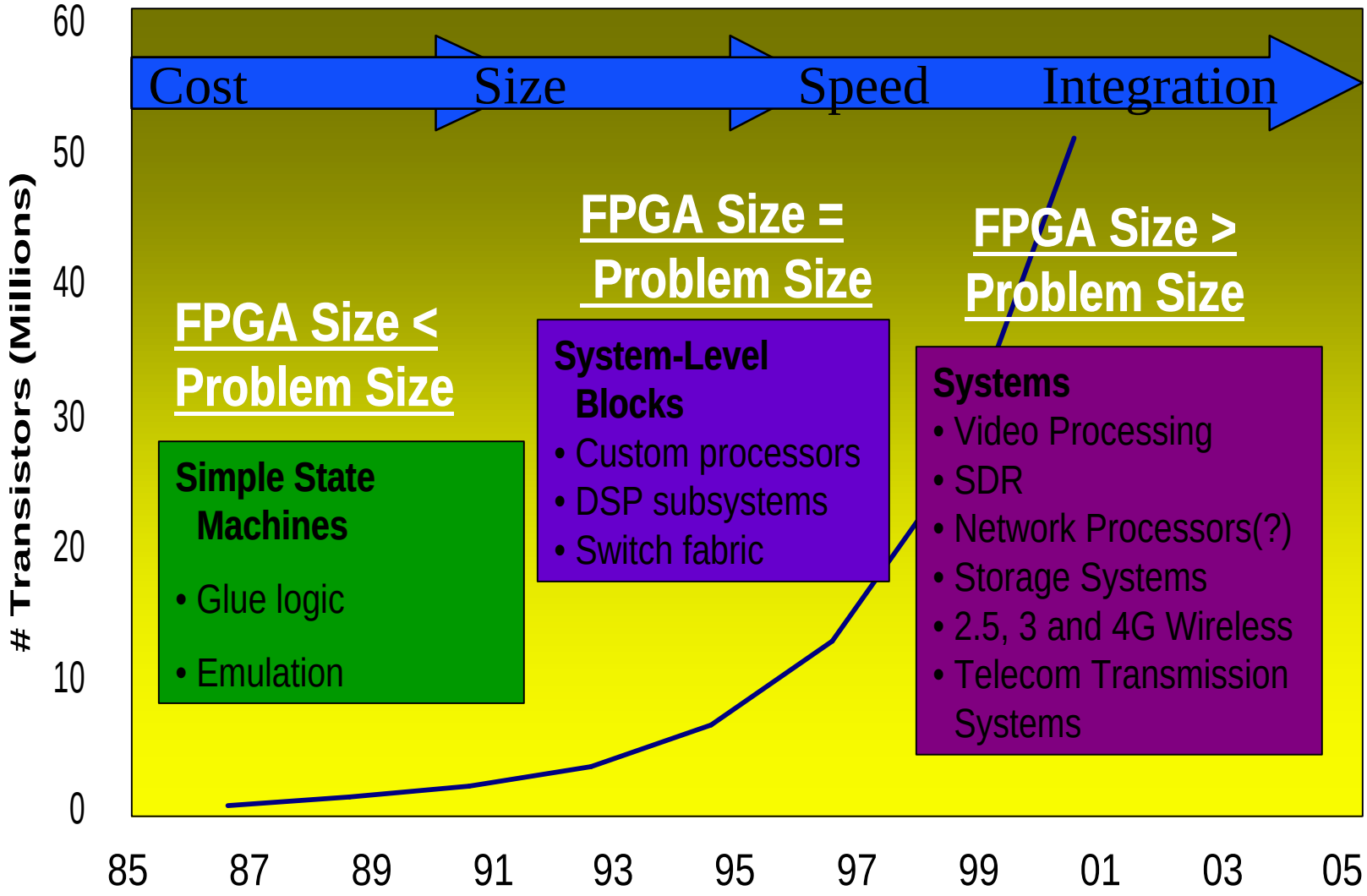
Alternative Interpretations of the Design Productivity Gap

1. Design methodology is falling behind.
   - We must make design more efficient
   - Higher-level capture; better automation
   - Eliminate the “Intelligent Designer”
2. The design problem is just too big for one person.
   - We must make design teams effective
3. Transistors are cheap.
   - Spend them for something more valuable (like design time)

Volume Manufacturing

- Need advanced CMOS process
  - Speed, capacity, cost
  - The most advanced is the simplest: transistors and wires
- Test is critical
  - Test is cheaper without non-volatile programming (er, how do you test matches anyway?)
  - BIST: leverage reconfigurability to test itself

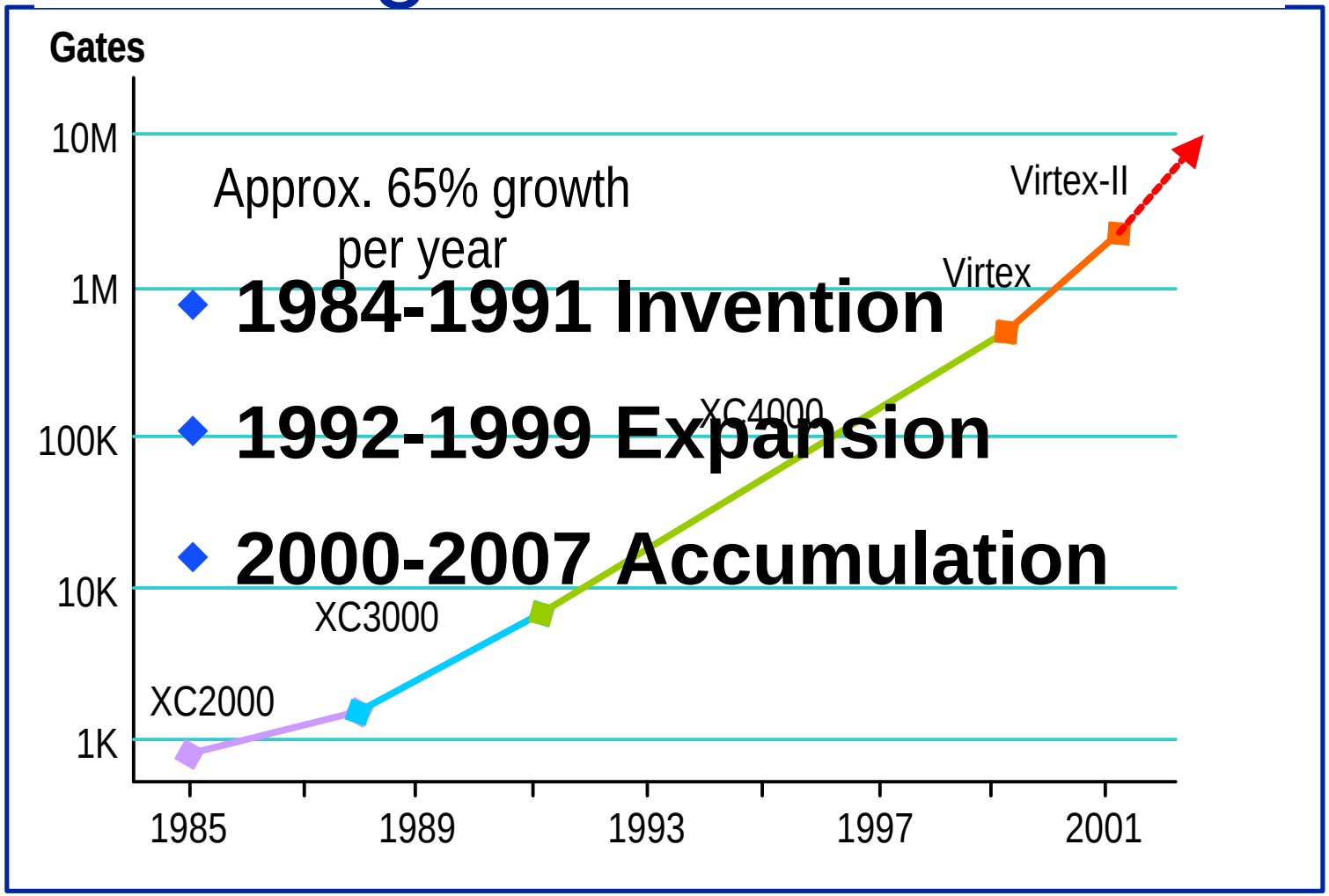
Applications Focus



FPGA Evolution

- Part 1. Environment
- **Part 2. Development**
  - The three Ages of FPGAs
  - Market-based Darwinian evolution
  - Extinction events
- Part 3. Focus on Reconfiguration
- Part 4. Looking Ahead

Development: The Three Ages of FPGAs



The Age of Invention

- The Pre-Cambrian
  - FPGAs crawl out of the sea (of gates)
  - FPGAs are much smaller than the application problem size
- The Cambrian Explosion
  - The architecture of the month
  - CLA, LCA, ERA, ACT, xPLD, TC, ORCA, CAL, CL, QL, Am, AT, CLi, CP, GF, MPA, ...

The Tertiary Period

Mass extinctions in the mid 90s

Xilinx: 8100, 620[illegible] 470[illegible]rizm, …

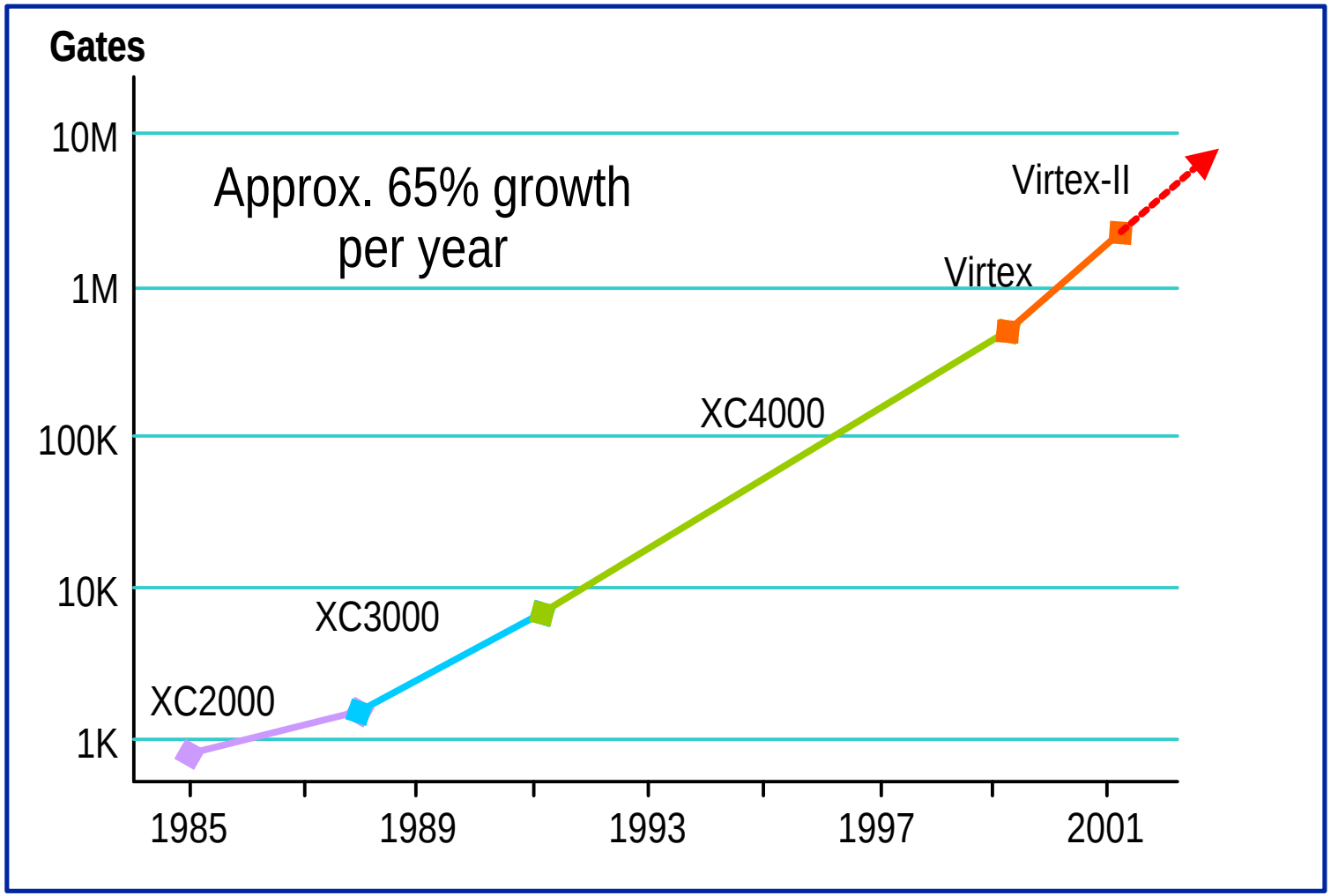
Plessey[illegible]oshib[illegible]a, IBM, …

We wer[illegible]

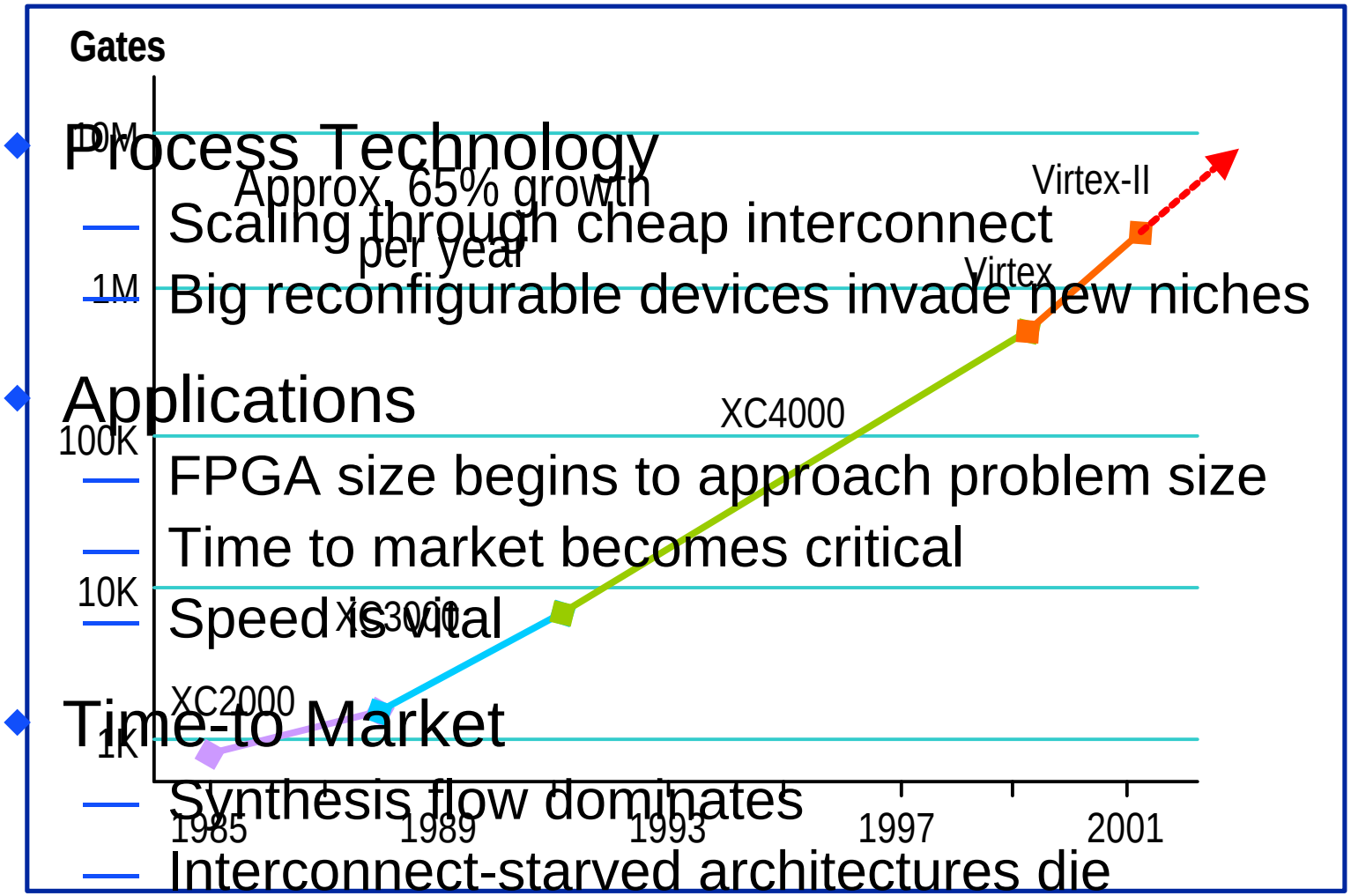
proce[illegible]

multi[illegible]

The Age of Expansion

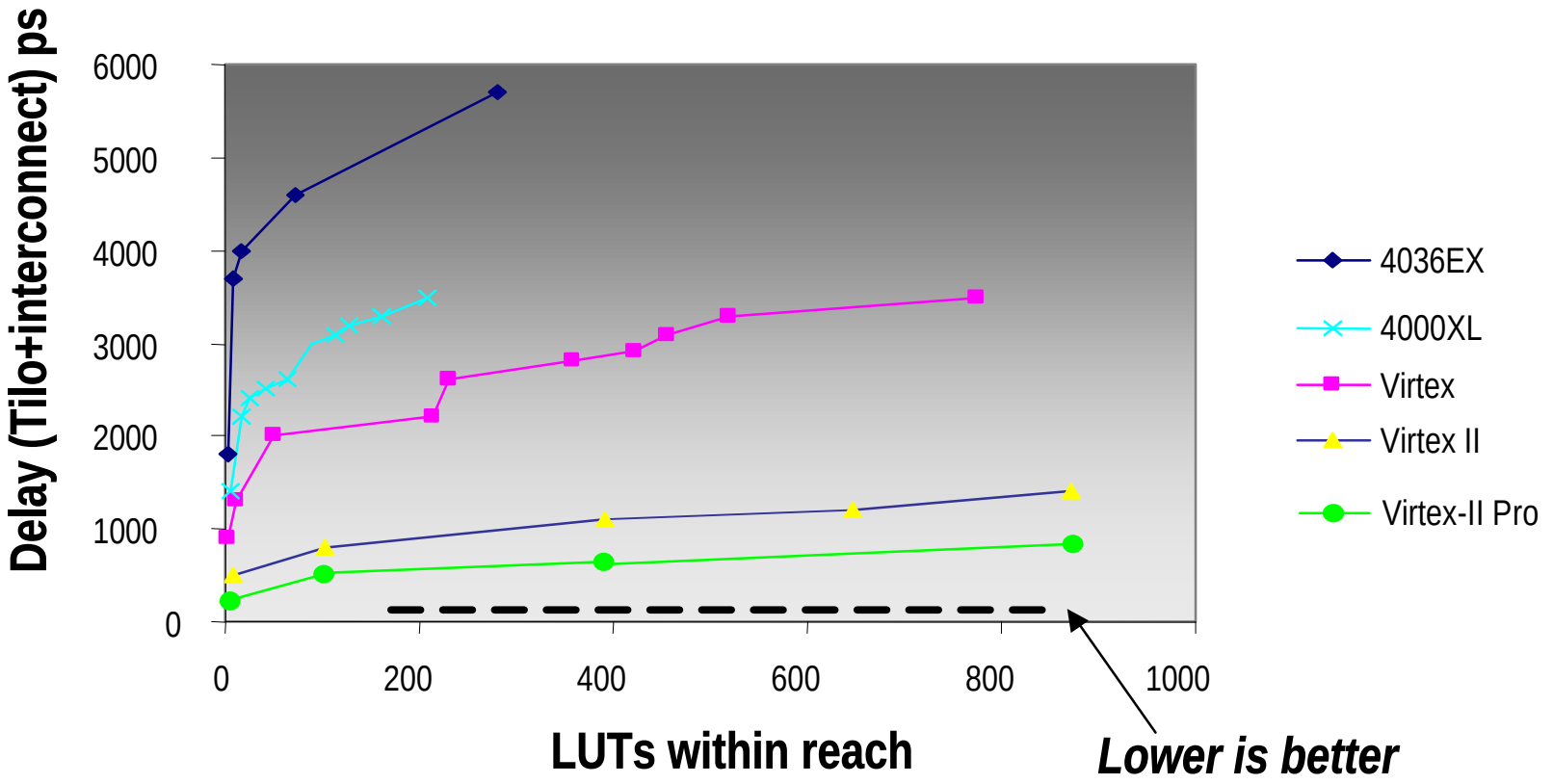


The Age of Expansion



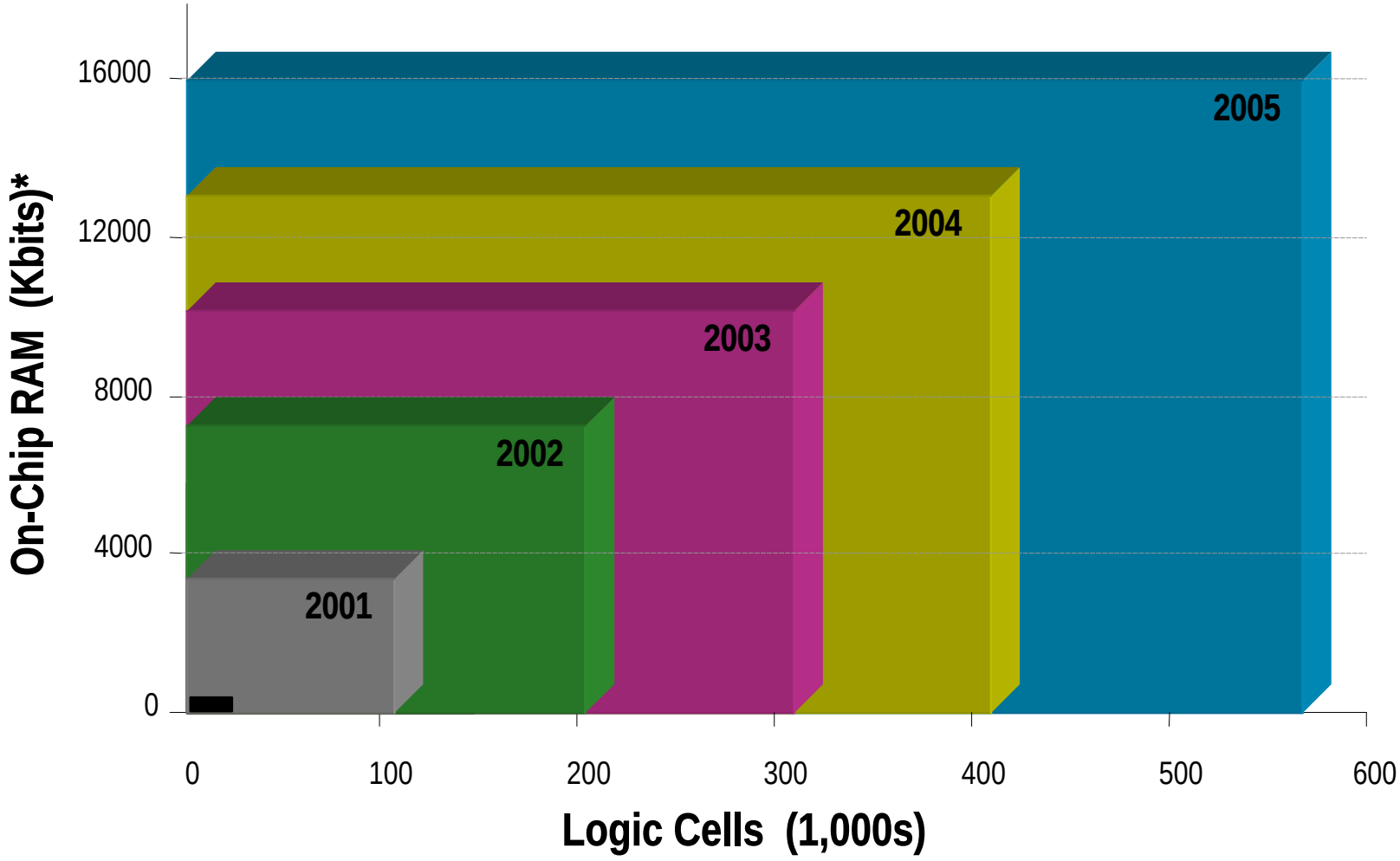
- Process Technology
  - Scaling through cheap interconnect
  - Big reconfigurable devices invade new niches
- Applications
  - FPGA size begins to approach problem size
  - Time to market becomes critical
  - Speed is vital
- Time-to Market
  - Synthesis flow dominates
  - Interconnect-starved architectures die

On-chip Performance Improvement



Dramatic improvement for "hands-off" design

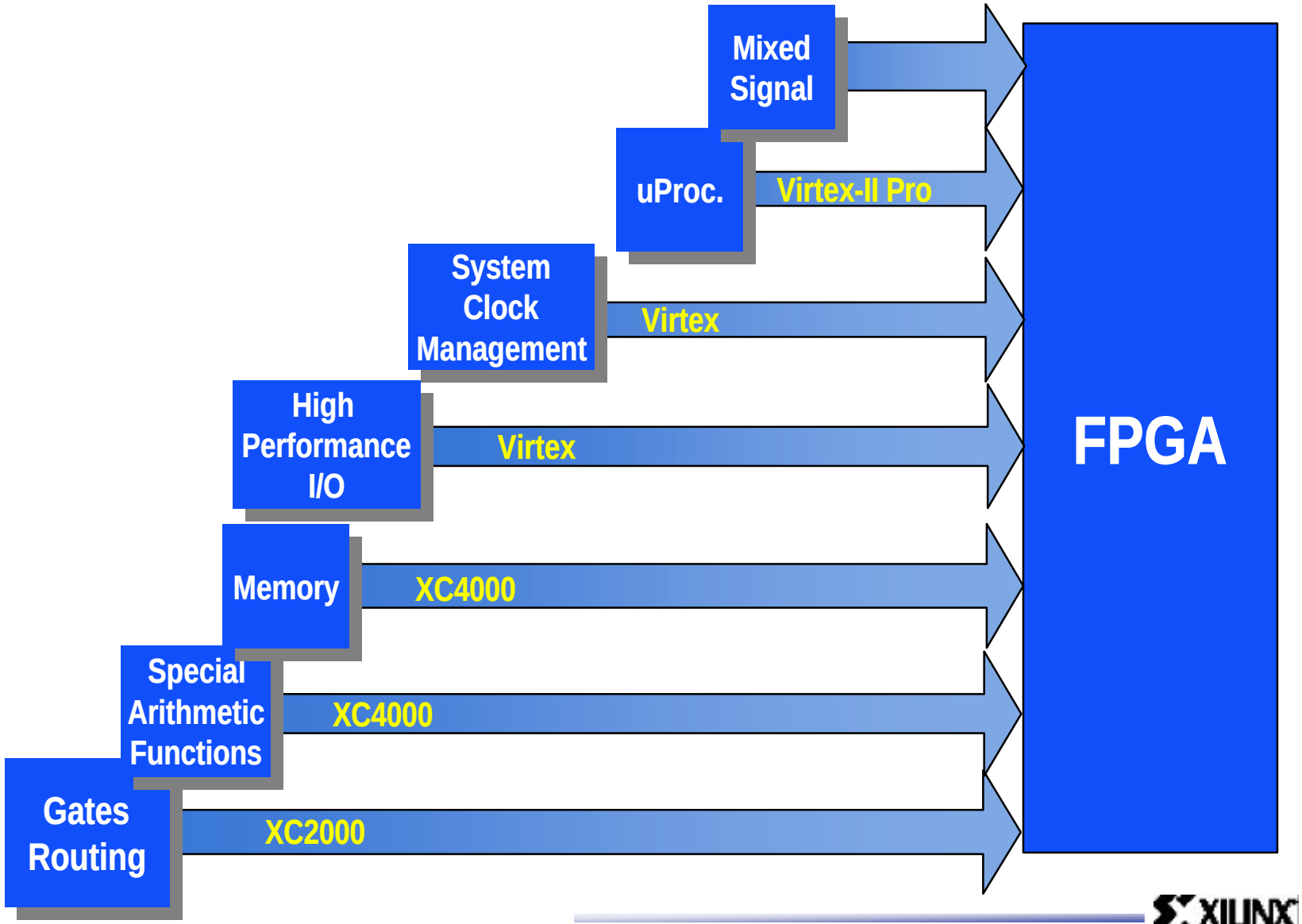
50 Million System Gates in 2005!



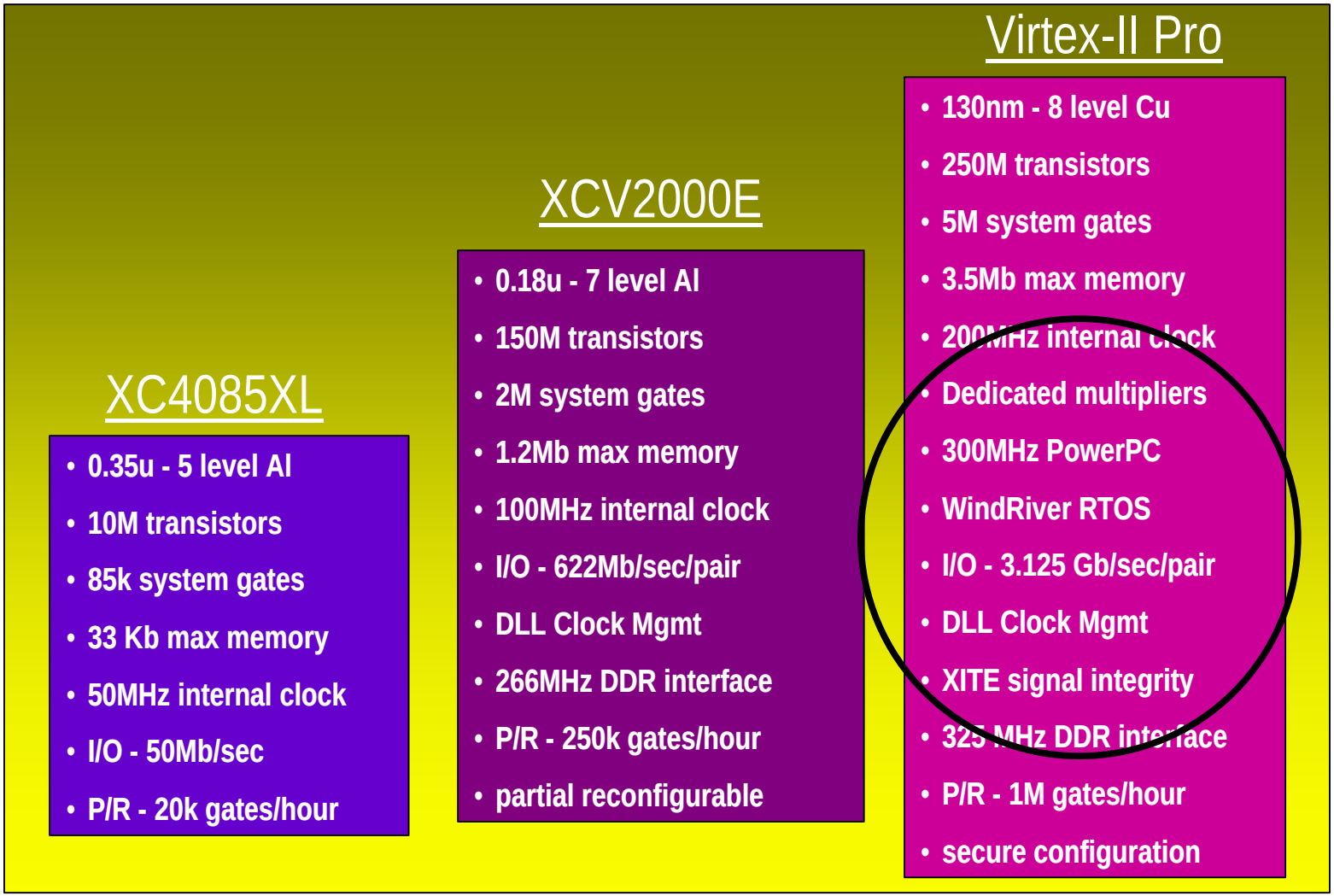
* assumes 25% of CLBs used as RAM

ST 7/18/2001

The Age of Accumulation



The Age of Accumulation



Evolutionary Pressures in the 21st Century

- Moore's Law
  - Continues for the foreseeable future
- Volume Manufacturing
  - Special structures for test and verification
- Time to market
  - Board-level systems issues
  - Signal integrity
  - How to use all the stuff?
  - Verification
- Applications demands
  - Power, signal integrity, reliability, speed

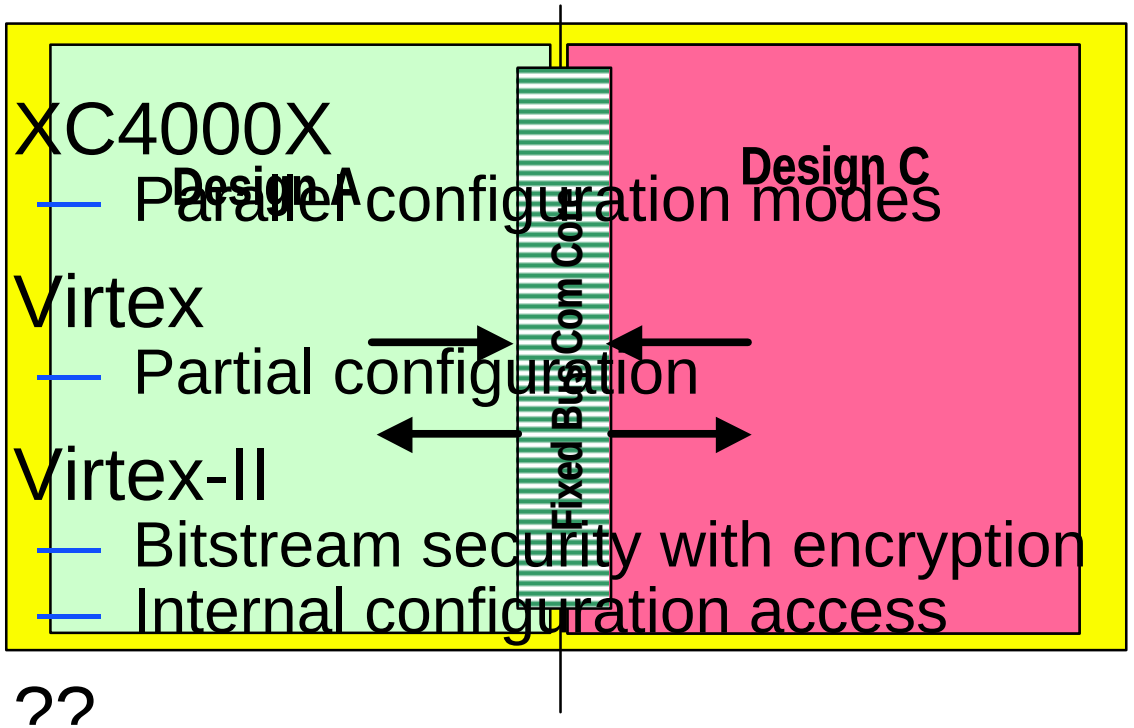
FPGA Evolution

- Part 1. Environment
- Part 2. Development
- **Part 3. Focus on Reconfiguration**
  - What is its survival advantage?
  - How are environmental pressures affecting it?
- Part 4. Looking Ahead

Reconfiguration Evolution

Supporting Process Technology and

Volume Manufacturing



- XC4000X
  - Parallel configuration modes
- Virtex
  - Partial configuration
- Virtex-II
  - Bitstream security with encryption
  - Internal configuration access
- ??
  - Addressable configuration
  - Contention-free partial reconfiguration

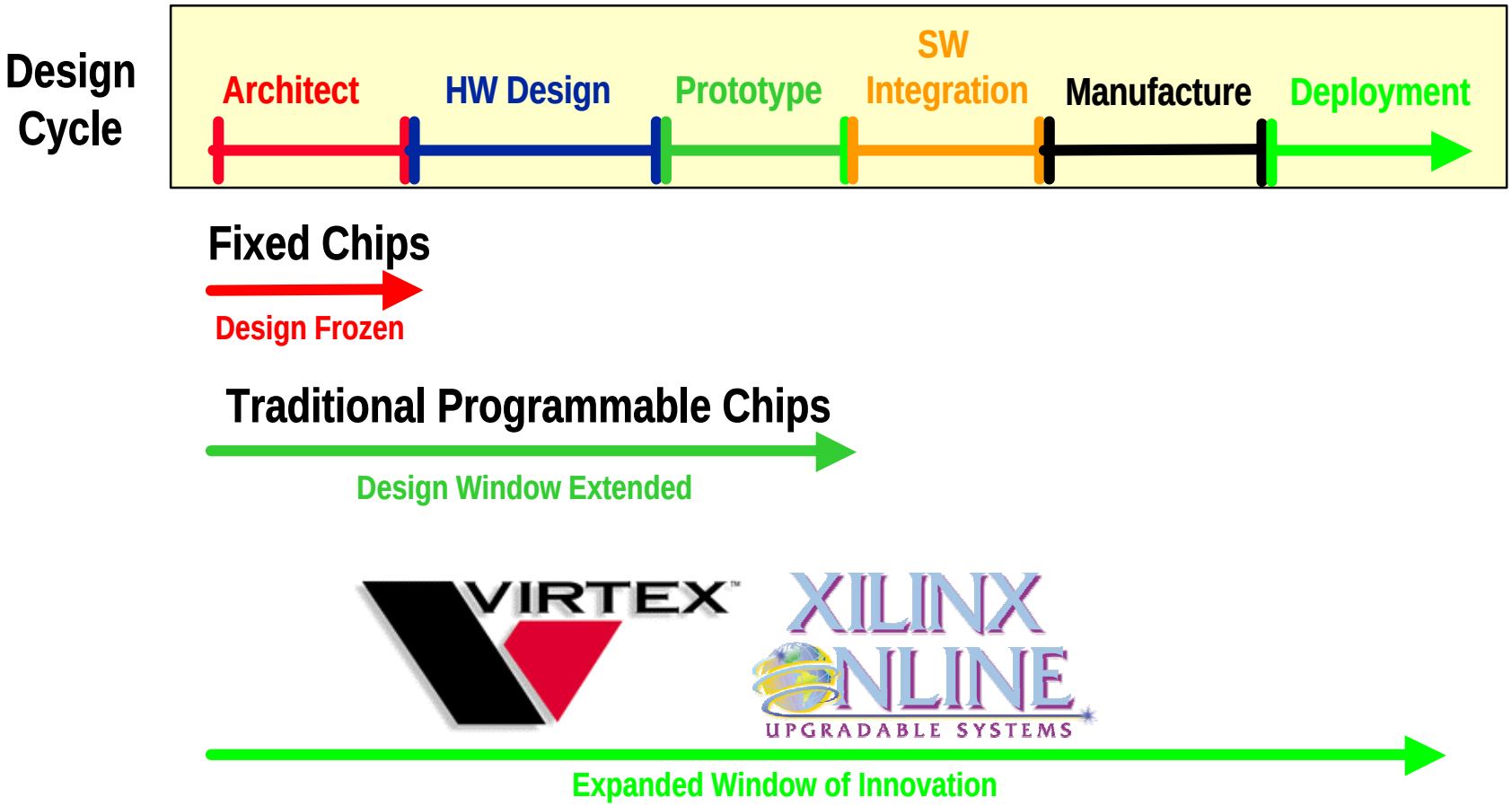
So What Happened to Rapid Reconfiguration?

- Not a competitive advantage in the 1990s
  - Configuration times were not fatally long
  - Very-high-speed configuration logic (ns) took too much space
  - Moderate-speed reconfiguration (microseconds) had marginal benefits
  - There were other ways to get done the tasks that were addressed by reconfiguration
  - Software was not in place to exploit it
- Bigger FPGAs simply out-competed rapidly-reconfigurable devices

What is Changing?

- Volume Manufacturing
  - Test time is dominated by configuration time
  - Configuration time scales with gate count
  - ⇒ Test time is getting long.
- Process Technology
  - Configuration architecture is changing as process technology causes long wires to be problematic
- Applications
  - High-speed, low C interconnect circuits

Applications and Time to Market
The Window of Innovation



FPGA Evolution

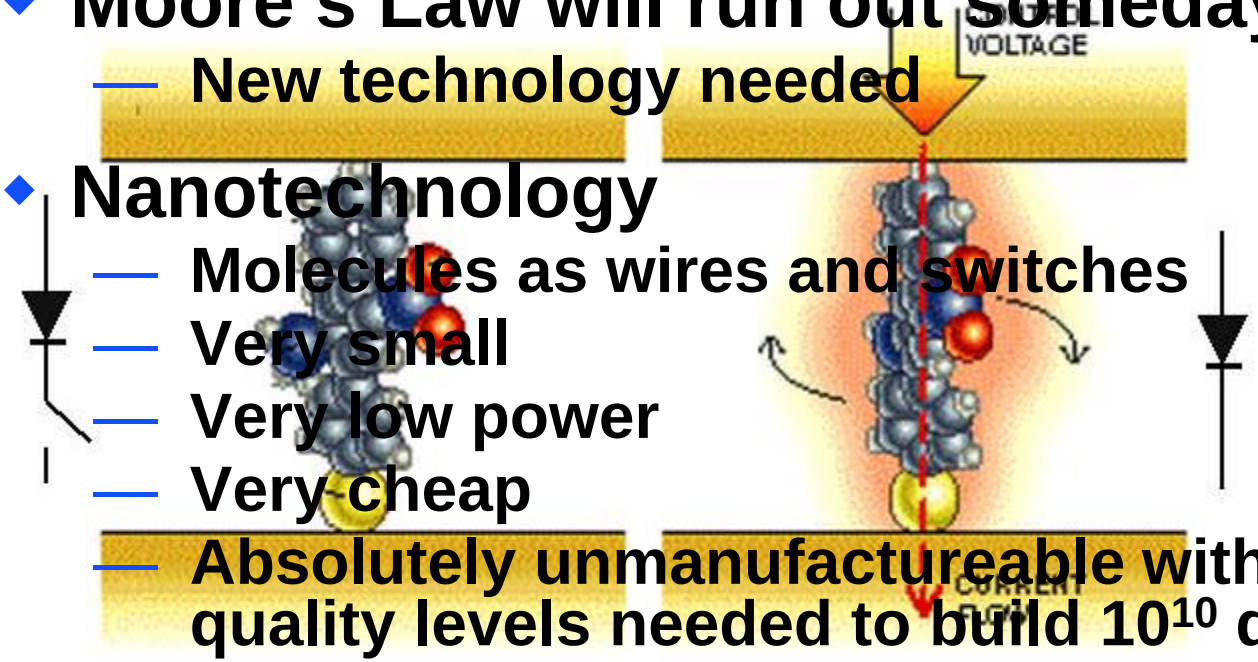
- Part 1. Environment
- Part 2. Development
- Part 3. Focus on Reconfiguration
- **Part 4. Looking Ahead**
  - A peek at the *end* of the 21st century

FPGA 2100

Line Width	100 pm
Wafer Size	2m
Die Size	25 cm^2
Transistor Count	2.5 x 10^{14}
FPGA Gate Count	1 B
Design Speed	60GHz
Power	200 KW
Fab Cost	$1T
Mask Set Cost	$1B
Design Time	5 *centuries*

Nanotechnology

- **Moore's Law will run out someday**
  - **New technology needed**
- **Nanotechnology**
  - **Molecules as wires and switches**
  - **Very small**
  - **Very low power**
  - **Very cheap**
  - **Absolutely unmanufactureable with the quality levels needed to build 10^{10} devices**
  - **Nanotechnology systems will need**



In Summary

- Environment pressure from process technology, volume manufacturing, applications and time-to-market
- Reconfiguration has been driven by process technology and manufacturability, not by applications
- Reconfiguration is now required for new models of delivery of functionality

So, what will be the fourth Age of FPGAs?